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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,058	04/08/2004	Takehiro Suzuki	1035-505	7339

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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 12/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/820,058	SUZUKI, TAKEHIRO	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on 07 Nov. 2005. These drawings are acceptable.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 6-7, 10 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6838769 to Chittipeddi et al.

Regarding claim 1, Chittipeddi discloses a semiconductor device in fig. 2, comprising: a semiconductor substrate 1, col. 3 line 12, having formed thereon a semiconductor element 7, col. 3 line 7, a first wiring layer 5, col. 3 line 34, formed on said semiconductor substrate 1 above an operating region (transistor 7) where said semiconductor element 7 is formed, said first wiring layer 5 being electrically connected to said operating region 7, fig. 2; a second wiring layer 19, col. 3 line 31, formed on said semiconductor substrate 1 above said first wiring layer 5; and a bonding pad 27, col. 3 line 9, to be electrically connected to an external connection terminal, fig. 2,

formed on said semiconductor substrate 1 above said second wiring layer 19, fig. 2, at least a part of said bonding pad 27 being located above said operating region 7, wherein said second wiring layer 19 includes a plurality of wirings 19, fig. 2, formed in the region under said bonding pad 27, a predetermined wiring 19 of said plurality of wirings 19 is connected to said bonding pad 27, fig. 2, and an insulating film 11, col. 3 line 28, is formed between other wirings 19 than the predetermined wiring 19 among said plurality of wirings 19, and the bonding pad 27; said other wirings 19 provided parallel to the edges of said bonding pad 27 are not formed in regions right under the edges, fig. 2; and said insulating film 8 is made up of an inorganic insulating film only, col. 5 line 16, so that no organic insulating film is provided between the other wiring 19 and the bonding pad 27.

Regarding claim 6, Chittipeddi discloses the semiconductor device wherein said bonding pad 27 is to be electrically connected to said inner lead by an inner lead bonding process, col. 4 line 27, and said other wirings 19 formed parallel to the edges of a region to be electrically connected to an inner lead on a surface of said bonding pad 27 are not formed in regions right under the edges fig. 2.

Regarding claim 7, Chittipeddi discloses a semiconductor device in fig. 2 comprising: a semiconductor substrate 1 having formed thereon a semiconductor element 7; a first wiring layer 5 formed on said semiconductor substrate 1 at above an operating region (transistor 7) where said semiconductor element 7 is formed, said first wiring layer 5 being electrically connected to said operating region 7; a second wiring layer 19 formed on said semiconductor substrate1 at above said first wiring layer 5;

and a bonding pad 27 to be electrically connected to an inner lead by an inner lead bonding process, col. 4 line 27, formed on said semiconductor substrate 1 at above said second wiring layer 19, at least a part of said bonding pad 27 being located right above said operating region, wherein said second wiring layer 19 includes a plurality of wirings 19 formed in the region right under said bonding pad 27, a predetermined wiring 19 of said plurality of wirings 19 is connected to said bonding pad 27, and an insulating film 11 is formed between other wirings 19 than the predetermined wiring 19 among said plurality of wirings, and the bonding pad 27; said other wirings 19 provided parallel to edges of said bonding pad 27 are not formed in regions right under the edges of the regions electrically connected to the inner lead on the surface of said bonding pad 27, fig. 2; and said insulating film 11 comprises an inorganic insulating film only, so that a bottom surface of the bonding pad 27 does not contact any organic insulating film, fig. 2.

Regarding claim 10, Chittipeddi discloses the semiconductor device wherein said insulating film 11 is made up of a silicone oxide film and a silicone nitride film, formed by the CVD, col. 5 line 16-18.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2-5, 8-9, and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chittipeddi in view of Applicant Admitted Prior Art (APA).

Regarding claims 2-3, 8-9, Chittipeddi discloses the semiconductor device wherein said other wirings 19 are not formed beyond the edge of the bonding pad 27, fig.2, said other wirings 19 being provided parallel to the edges of bonding pad 27 and the bonding pad in under stress by inner bonding process, col. 4 lines 14-17.

But Chittipeddi does not expressly discloses the in expanded regions right under said expanded regions as expanded with a stress in a process of electrically connecting said bonding pad to an external connection terminal, wherein respective lengths of the expanded regions in the expanding direction of said bonding pad are set to fall in a range of from 2 micron to 3 micron.

However, APA discloses in fig. 9 a semiconductor device comprises a wire 202 having bonding pad 201, an expanded regions right under said expanded regions 201a-b as expanded with a stress in a process of electrically connecting said bonding pad to an external connection terminal 208, fig. 9, wherein respective lengths of the expanded regions in the expanding direction of said bonding pad 201 are set to fall in a range of from 2 micron, see background of the invention in fig. 9. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to conclude that the bonding pad 27 of Chittipeddi would have the expanded regions as claimed. Where the claimed and the prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a

prima facie case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977).

Regarding claims 4-5, Chittipeddi does not disclose the semiconductor device wherein said bonding pad 27 and said external connection terminal are electrically connected by the chip-on-glass or chip-on board.

However, APA discloses the semiconductor device wherein bonding pad 201 and said external connection terminal are electrically connected by the chip-on-glass (COG) or TCP, see background of the invention. At the time the invention was made; it would have been obvious to one of ordinary skill in the use the teaching of APA with Shimizu for intended use because the recitation 'chip-on-glass' or 'chip-on-board' of the claimed invention does not result in a structural difference between the claimed invention and the prior art, thus claimed invention is only an art recognized suitability for an intended purpose, MPEP 2144.07.

Regarding claim 11, Chittipeddi discloses a semiconductor device in fig. 2, comprising: a semiconductor substrate 1 having formed thereon a semiconductor element 2; a first wiring layer 5 formed on said semiconductor substrate 1 at above an operating region where said semiconductor element 7 is formed, said first wiring layer 5 being electrically connected to said operating region; a second wiring layer 19 formed on said semiconductor substrate 1 at above said first wiring layer 5; and a bonding pad 27 to be electrically connected to an external connection terminal, fig. 2, formed on said semiconductor substrate 1 at above said second wiring layer 5, at least a part of

said bonding pad 27 being located right above said operating region, wherein said second wiring layer 19 includes a plurality of wirings 19, a predetermined wiring 19 of said plurality of wirings is connected to said bonding pad 27, and an insulating film 11 is formed between other wirings 19 than the predetermined wiring 19 among said plurality of wirings, and said bonding pad 27; said other wirings 19 are formed so as to avoid regions right under the edges in the lengthwise direction of said bonding pad 27 and said insulating film includes an inorganic insulating film, so that no organic insulating film is provided between the other wiring 19 and the bonding pad 27, fig. 2.

But Chittipeddi does not expressly disclose under the edges in the lengthwise direction of bonding pad to 3 micron outside the region.

However, Chittipeddi clearly discloses a general distance from the edge of the bonding pad 27 to the second wire layer 19. Accordingly, it would have been obvious to one of ordinary skill in art to use the general distance teaching of Chittipeddi in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

Regarding claim 12, Chittipeddi discloses the semiconductor device wherein said insulating film 11 is made up of an inorganic insulating film only.

Regarding claim 13, Chittipeddi discloses the semiconductor device wherein at least a part of said other wirings 19 is formed in a region right under said bonding pad 27, and other wirings 19 formed in the region right under the bonding pad 27 are

formed only in a region right under a region electrically connected to an inner lead on a surface of said bonding pad, fig. 2.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le
30 November 2005

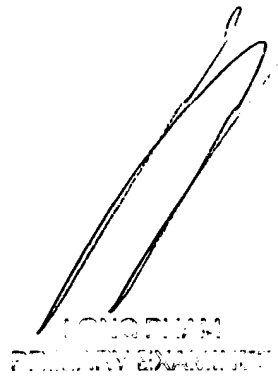

FIG. 7 (a) (Prior Art)

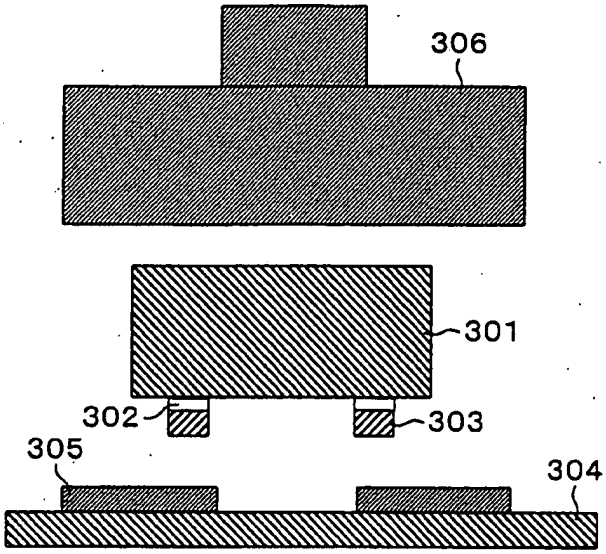

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FIG. 7 (b) (Prior Art)

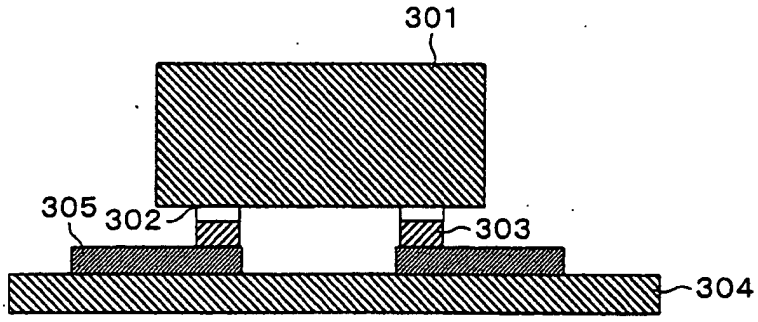

FIG. 8 (Prior Art)

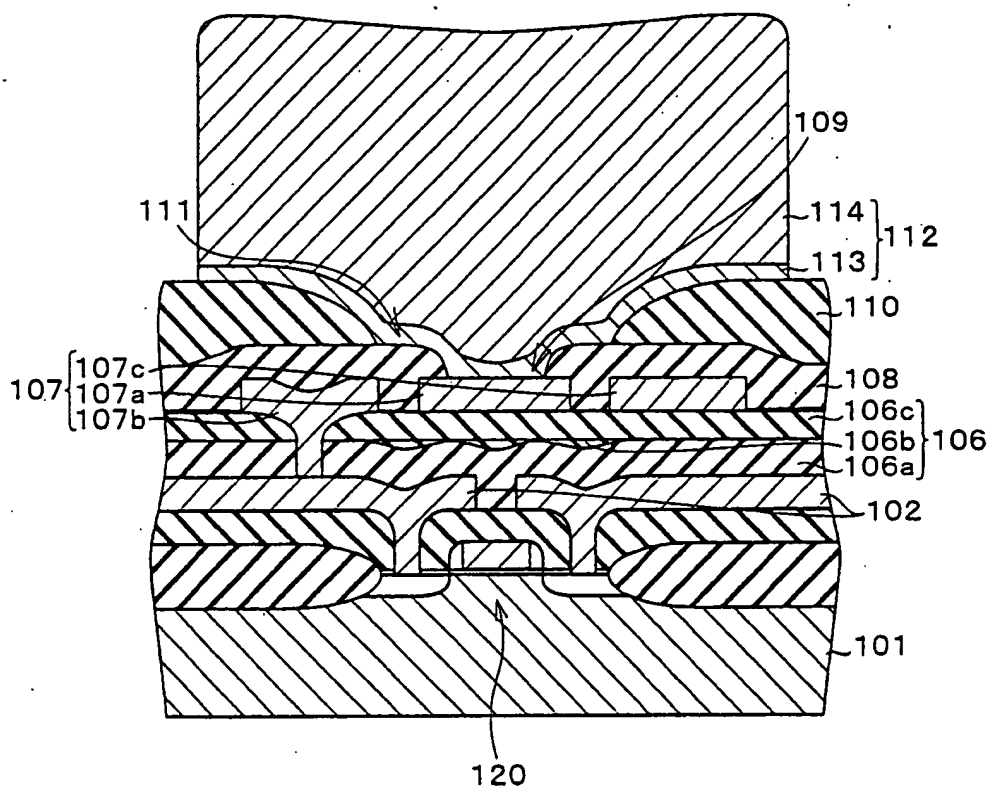

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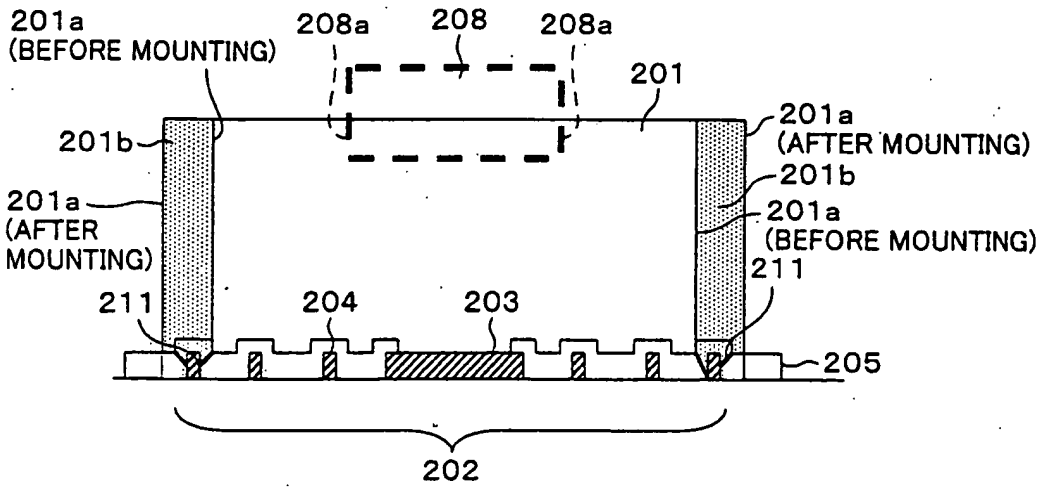
FIG. 9 (Prior Art)



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